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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
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10/685,177

10/14/2003

Andrew Harvey Barr

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05/31/2007

HEWLETT PACKARD COMPANY

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INTELLECTUAL PROPERTY ADMINISTRATION

FORT COLLINS, CO 80527-2400

EXAMINER

MERANT, GUERRIER

ART UNIT

PAPER NUMBER

2117

MAIL DATE

DELIVERY MODE

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PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

The time period for reply, if any, is set in the attached communication.

Office Action Summary

Application No.

10/685,177

Applicant(s)

BARR ET AL.

Examiner

Guerrier Merant

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-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

- 1) ☒ Responsive to communication(s) filed on 14 October 2003.
- 2a) ☐ This action is **FINAL**. 2b) ☒ This action is non-final.
- 3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

- 4) ☒ Claim(s) 1-21 is/are pending in the application.
- 4a) Of the above claim(s) _____ is/are withdrawn from consideration.
- 5) ☐ Claim(s) _____ is/are allowed.
- 6) ☒ Claim(s) 1-21 is/are rejected.
- 7) ☐ Claim(s) _____ is/are objected to.
- 8) ☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

- 9) ☐ The specification is objected to by the Examiner.
- 10) ☒ The drawing(s) filed on 14 October 2003 is/are: a) ☒ accepted or b) ☐ objected to by the Examiner.
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).
- 11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

- 12) ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
- a) ☐ All b) ☐ Some * c) ☐ None of:
- ☐ Certified copies of the priority documents have been received.
 - ☐ Certified copies of the priority documents have been received in Application No. _____.
 - ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).
- * See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

- | | |
|---|---|
| 1) ☒ Notice of References Cited (PTO-892) | 4) ☐ Interview Summary (PTO-413)
Paper No(s)/Mail Date. _____ |
| 2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948) | 5) ☐ Notice of Informal Patent Application |
| 3) ☒ Information Disclosure Statement(s) (PTO/SB/08)
Paper No(s)/Mail Date <u>10/14/03</u> . | 6) ☐ Other: _____ |

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DETAILED ACTION

This is the initial Office Action based on the application filed on October 14, 2003.

Claims 1-20 are currently pending and have been considered below.

Claim Rejections - 35 USC § 112

The following is a quotation of the second paragraph of 35 U.S.C. 112:

The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter, which the applicant regards as his invention.

Claims 1 & 12 are rejected under 35 U.S.C. 112, second paragraph, as being incomplete for omitting essential steps, such omission amounting to a gap between the steps. See MPEP § 2172.01.

As per claims 1 and 12:

It is not clear to the Examiner how the compiling is performed by opportunistically scheduling diagnostic testing of CPU registers.

Claim Rejections - 35 USC § 101

35 U.S.C. 101 reads as follows:

Whoever invents or discovers any new and useful process, machine, manufacture, or composition of matter, or any new and useful improvement thereof, may obtain a patent therefor, subject to the conditions and requirements of this title.

Claim 12 is rejected under 35 U.S.C. 101 because the claimed invention is directed to non-statutory subject matter.

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As per claim 12, the claim fails to fall within a statutory category by reciting " a computer- readable program for execution on a target microprocessor".

The Examiner suggests that the "program" be embedded in a computer readable medium.

Appropriate correction is required.

Claim Rejections - 35 USC § 102

The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

Claims 1 & 12 are rejected under 35 U.S.C. 102(e) as being anticipated by **Barto et al. (US 7,127,310 B1)**.

Claim 1: **Barto** discloses a method of compiling a program to be executed on a target central processing unit (CPU) (*e.g. items 110, fig. 1*), the method comprising opportunistically scheduling diagnostic testing of CPU registers (*e.g. col. 7, lines 24-60*).

Claim 12: **Barto** discloses a computer-readable program product for execution on a target microprocessor (*e.g. items 110, fig. 1*), the program product comprising

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executable code configured to opportunistically schedule diagnostic testing of registers in the microprocessor (*e.g. col. 7, lines 24-60*).

Claims 1-3, 6, 12-14 & 21 are rejected under 35 U.S.C. 102(e) as being anticipated by **Quach (US 6,640,313 B1)**.

Claim 1: **Quach** discloses a method of compiling a program to be executed on a target central processing unit (CPU) (*e.g. col. 4, lines 46-53, fig. 1*), the method comprising opportunistically scheduling diagnostic testing of CPU registers (*col. 2, lines 32-41; instructions are provided by an issue module to processor's modes which are scheduling to run a diagnostic code in HR mode or scheduling to run program code in HP mode; running instructions on a processor in HR mode is interpreted as selecting such processor*).

Claim 2: **Quach** discloses a method as in claim 1 above, further comprising: checking a predetermined level of aggressiveness for the scheduling of the register diagnostic testing (*col. 2, lines 43-50; a check unit is activated in HR mode or deactivated in HP mode by compare executing result*).

Claim 3: **Quach** discloses a method as in claim 2 above, further comprising: determining a next register to be tested (*e.g. col. 11, lines 8-40*).

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Claim 6: Quach discloses a method as in claim 1 above, wherein the CPU registers comprise registers in a general register file (*inherent; all processing systems comprise register files*).

Claim 12: Quach discloses a computer-readable program product for execution on a target microprocessor (*e.g. col. 4, lines 46-53, fig. 1*), the program product comprising executable code configured to opportunistically schedule diagnostic testing of registers in the microprocessor (*col. 2, lines 32-41; instructions are provided by an issue module to processor's modes which are scheduling to run a diagnostic code in HR mode or scheduling to run program code in HP mode; running instructions on a processor in HR mode is interpreted as selecting such processor*).

Claims 13 & 21: Quach discloses a computer-readable program product as in claim 12 above, further comprising executable code configured to check a predetermined level of aggressiveness for the scheduling of the register diagnostic testing (*col. 2, lines 43-50; a check unit is activated in HR mode or deactivated in HP mode by compare executing result*).

Claim 14: Quach discloses a computer-readable program product as in claim 13 above, further comprising executable code configured to determine a next register to be tested (*e.g. col. 11, lines 8-40*).

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Claim Rejections - 35 USC § 103

The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

(a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negated by the manner in which the invention was made.

Claims 7-10, 17-20 are rejected under 35 U.S.C. 103(a) as being unpatentable over

Quach as applied to claim 1 above, and further in view of Raina (US 6, 134, 675).

As per claims 7 & 17: Quach fails to teach writing known data to a register, reading data from the register, and comparing the known data with the data that was read but Raina teaches the scheduled diagnostic code performs diagnostic operations from a test pattern comprising comparing an actual result with known expected results (col.3 lines 19-22). Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Quach's teachings the scheduled diagnostic code by performing diagnostic operations from a test pattern comprising operations with known expected results as taught by Raina in order to improve method that is better suited for testing integrated circuits containing multiple core

As per claims 8, 10, 18 & 20: Quach in view of Raina teach a method/ a computer-readable program of claims 7 & 17 above, wherein if the comparison indicates a difference, then jumping to a fault handler routine (e.g. col. 3, lines 15-22; Raina).

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As per claims 9 & 19: Quach in view of Raina teach a method/ a computer-readable program as in claims 8 and 18 above, wherein the fault handler routine is configured to halt execution to avoid potential data corruption (e.g. col. 3, lines 17-19; Raina).

Claim 11 is rejected under 35 U.S.C. 103(a) as being unpatentable over Barto et al. and further in view of Schreiber (US 6,460,173 B1).

As per claim 11: But Barto et al. fails to teach determining if there is sufficient opportunity to schedule a register diagnostic instruction to test the next register; if there is sufficient opportunity, then scheduling the register diagnostic instruction to test the next register; and if there is insufficient opportunity, then scheduling user code instructions. However, Schreiber teaches *a method and apparatus for selecting operation devices or hardware components for a processor comprising an initiation interval for that determines if there is sufficient cycle time to perform a specific instruction and if the cycle time is insufficient assign adjust the time in order to execute the instructions* (e.g. col. 5, lines 53-67 & col. 6, lines 1-18).

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use in the method of Barto et al. the initiation interval taught by Schreiber in order to reduce the time required for designing processors, and reduce the amount of trial and error used in processor design (e.g. col. 2, lines 24-30; Schreiber).

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Claims 4, 5, 11 & 15-16 are rejected under 35 U.S.C. 103(a) as being unpatentable over Quach and further in view of Schreiber (US 6,460,173 B1).

As per claims 4-5 & 15-16: Quach fails to teach if there is sufficient opportunity, then scheduling the register diagnostic instruction to test the next register; and if there is insufficient opportunity, then scheduling user code instructions. However, Schreiber teaches *a method and apparatus for selecting operation devices or hardware components for a processor comprising an initiation interval for that determines if there is sufficient cycle time to perform a specific instruction and if the cycle time is insufficient assign adjust the time in order to execute the instructions (e.g. col. 5, lines 53-67 & col. 6, lines 1-18).*

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use in the method of Quach the initiation interval taught by Schreiber in order to reduce the time required for designing processors, and reduce the amount of trial and error used in processor design (e.g. col. 2, lines 24-30; Schreiber).

Claim 11: Quach substantially teaches a method of compiling a program to be executed on a target central processing unit (CPU) (e.g. col. 4, lines 46-53, fig. 1), the method comprising: opportunistically scheduling diagnostic testing of CPU registers (col. 2, lines 32-41; *instructions are provided by an issue module to processor's modes which are scheduling to run a diagnostic code in HR mode or scheduling to run program code in*

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HP mode; running instructions on a processor in HR mode is interpreted as selecting such processor);

checking a predetermined level of aggressiveness for the scheduling of the register diagnostic testing; determining a next register to be tested (*col. 2, lines 43-50; a check unit is activated in HR mode or deactivated in HP mode by compare executing result*).

But Quach fails to teach determining if there is sufficient opportunity to schedule a register diagnostic instruction to test the next register; if there is sufficient opportunity, then scheduling the register diagnostic instruction to test the next register; and if there is insufficient opportunity, then scheduling user code instructions. However, Schreiber teaches *a method and apparatus for selecting operation devices or hardware components for a processor comprising an initiation interval for that determines if there is sufficient cycle time to perform a specific instruction and if the cycle time is insufficient assign adjust the time in order to execute the instructions (e.g. col. 5, lines 53-67 & col. 6, lines 1-18)*.

Therefore, at the time the invention was made, it would have been obvious to a person of ordinary skill in the art to use in the method of Quach the initiation interval taught by Schreiber in order to reduce the time required for designing processors, and reduce the amount of trial and error used in processor design (e.g. col. 2, lines 24-30; Schreiber).

Conclusion

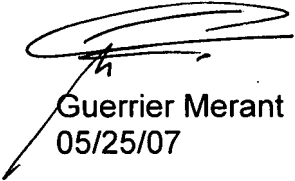
Any inquiry concerning this communication or earlier communications from the examiner should be directed to Exr. Merant Guerrier whose telephone number is (571)

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270-1066. The examiner can normally be reached Monday through Thursday from 10:30 a.m. to 3:30 p.m.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jacques Louis Jacques, can be reached on (571) 272-6962. Draft or Informal faxes, which will not be entered in the application, may be submitted directly to the examiner at (571) 270-2066.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.



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05/25/07



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